REMARKS

Claims 52, 55, 61, 69, 72, and 75 are amended, claims 56, 70, 71, 73, 74, 76, and 77 are canceled, and no claims are added; as a result, claims 22-55, 57-69,72, and 75 are now pending in this application.

§112 Rejection of the Claims

Claims 22-77 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Office Action states that "the claims do not specifically require that it is the transistor itself that is acting to reduce the applied voltage." Applicant respectfully traverses.

Respectfully, applicant traverses this rejection on grounds that the claims are not indefinite. Specifically, in making the rejection the Examiner appears to treat the deliberate omission of particular implementation details from the rejected claims as indicative of indefiniteness, instead of claim scope. MPEP 2173.04 teaches that breadth or scope is distinct from indefiniteness, which generally relates to lack of clarity, such as vagueness or ambiguity, in the claim language itself. Further, this section states that "where the scope of the claim is clear and applicant has not otherwise indicated the invention is of a scope different from that defined in the claims, the claims comply with 35 USC 112, second paragraph.

In the rejected claims, the Examiner is correct in pointing out that applicant has omitted certain details. However, these omissions unambiguously signal that the scope of the claim is not limited by the specific nature. Thus, because the current claim language accurately and with reasonable certainty reflects the absence of further limitations on the control connection and the control effect, the current claim language is definite under 35 USC 112, second paragraph.

Applicant further submits that claim 22 meets the requirements of 35 USC 112, second paragraph as it provides the steps necessary for an embodiment of the invention , namely, applying the voltage to a transistor, reducing the voltage by a threshold voltage of the transistor; and providing the voltage reduced by the threshold voltage of the transistor at an output of the transistor, wherein the output of the transistor is coupled to a well that bounds the transistor.

Accordingly, applicant requests respectfully that the Examiner reconsider and withdraw the §112 rejections.

§102 Rejection of the Claims

Claims 22-77 were rejected under 35 USC § 102(e) as being anticipated by Nishio et al. Applicant respectfully traverses.

Claim 22 recites, in part, providing the voltage reduced by the threshold voltage of the transistor at an output of the transistor, wherein *the output of the transistor is coupled to a well that bounds the transistor* [italics added]. Applicant can not find these features in Nishio. As all of the features of claim 22 are not found in Nishio, applicant submits that claim 22 and dependent claims 23-26 are allowable.

The Office Action states that the integrated configuration of the Nishio circuit also results in the use of well regions which are also biased with the transistors, as well. Applicant can not find any teaching of such a feature in Nishio. More particularly, applicant can not find where Nishio explicitly discusses its wells containing its transistors. Clarification is requested.

Claim 27 recites, in part, providing the voltage reduced by the threshold voltage of the transistor at a second source/drain of the transistor and a well bounding the transistor. Applicant can not find this feature in Nishio. As all of the features of claim 27 are not found in Nishio, applicant submits that claim 27 and dependent claims 28-29 are allowable.

Claim 30 recites, in part, coupling a well, that isolates the transistor from a substrate, to the circuit. Applicant can not find this feature in Nishio. As all of the features of claim 30 are not found in Nishio, applicant submits that claim 30 and dependent claims 31-33 are allowable.

Claim 34 recites, in part, providing the voltage reduced by the threshold voltage of the transistor at a second source/drain of the transistor, *wherein a semiconductor region containing the first and second source/drains is coupled to the second source/drain of the transistor* [italics added]. Applicant can not find this feature in Nishio. As all of the features of claim 34 are not found in Nishio, applicant submits that claim 34 and dependent claims 35-37 are allowable.

Claim 38 recites, in part, isolating the transistor from a substrate region of the integrated circuit by a well formed in the substrate region; and coupling the well to the internal circuit.

Applicant can not find this feature in Nishio. As all of the features of claim 38 are not found in Nishio, applicant submits that claim 38 and dependent claims 39-40 are allowable.

Claim 41 recites, in part, providing the reduced voltage an output of the second transistor, wherein a well, bounding the first transistor and the second transistor, is coupled to the output. Applicant can not find this feature in Nishio. As all of the features of claim 41 are not found in Nishio, applicant submits that claim 41 and dependent claims 42-43 are allowable.

Claim 45 recites, in part, providing the reduced voltage at an output of the second transistor, wherein a first well, bounding the first transistor, is coupled to the second transistor and a second well, bounding the second transistor, is coupled to the output. Applicant can not find this feature in Nishio. As all of the features of claim 45 are not found in Nishio, applicant submits that claim 45 and dependent claims 46-48 are allowable.

Claim 49 recites, in part, providing the reduced voltage at a second source/drain of the second transistor, wherein the voltage is reduced by a threshold voltage of both the first transistor and the second transistor. Applicant can not find this feature in Nishio. As all of the features of claim 49 are not found in Nishio, applicant submits that independent claim 49 and dependent claims 50-51 are allowable.

Claim 52 recites, in part, providing the reduced voltage at a second source/drain of the second transistor, wherein the voltage is reduced by a threshold voltage of both the first transistor and the second transistor. Applicant can not find this feature in Nishio. As all of the features of claim 52 are not found in Nishio, applicant submits that independent claim 52 and dependent claims 53-54 are allowable.

Claim 55 recites, in part, a semiconductor region of the transistor containing the first and second source/drains is coupled to the node. Applicant can not find this feature in Nishio. As all of the features of claim 55 are not found in Nishio, applicant submits that independent claim 55 and dependent claims 57-60 are allowable.

Claim 61 recites, in part, biasing a well of the transistor to a second source/drain. Applicant can not find this feature in Nishio. As all of the features of claim 61 are not found in Nishio, applicant submits that independent claim 61 and dependent claims 62-64 are allowable.

Claim 65 recites, in part, providing the reduced voltage at an output of the transistor, wherein the output of the transistor is coupled to a well that isolates the transistor from a

substrate of the integrated circuit. Applicant can not find these features in Nishio. As all of the features of claim 65 are not found in Nishio, applicant submits that independent claim 65 and dependent claims 66-68 are allowable.

Claim 69 recites, in part, applying the reduced voltage to the at least one internal circuit, wherein a well that isolates the transistor from a substrate of the integrated circuit is coupled to the at least one internal circuit. Applicant can not find these features in Nishio. As all of the features of claim 69 are not found in Nishio, applicant submits that independent claim 69 is allowable.

Claim 72 recites, in part, providing the reduced voltage at a second source/drain of the second transistor; and applying the reduced voltage to the at least one internal circuit, wherein a semiconductor region containing the first and second source/drains and common source/drain of the first and second transistors is coupled to the at least one internal circuit. Applicant can not find these features in Nishio. As all of the features of claim 72 are not found in Nishio, applicant submits that independent claim 72 is allowable.

Claim 75 recites, in part, applying the reduced voltage to the at least one internal circuit, wherein a first semiconductor region containing the first and second source/drains of the first transistor is coupled to the first source/drain and the gate of the second transistor and wherein a second semiconductor region containing the first and second source/drains of the second transistor is coupled to the at least one internal circuit. Applicant can not find these features in Nishio. As all of the features of claim 75 are not found in Nishio, applicant submits that independent claim 75 is allowable.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-349-9587) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

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Date 9 July '03

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 9th day of July, 2003.

Amy Moriarty
Name

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Signature